Notice of Allowability	Application No.	Applicant(s)	
	10/721,316	CITRON, DANIEL	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/16/2006*.

2. ☒ The allowed claim(s) is/are *1-12 and 14-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Remarks filed on November 13, 2006 regarding application 10/721,316 filed on November 25, 2003.

2. Claims 1-12 and 14-25 are pending for consideration.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. Authorization for this examiner's amendment was given in a telephone interview with Suzanne Erez (Reg. No. 46,688) on 11/28/2006.

The application has been amended as follows:

- **The 3rd paragraph of Claim 1 is now amended to be**:

"a Level 1 (L1) cache and a Level 2 (L2) cache on the chip, which are arranged to store data for use by the processing component responsively to an addressing scheme based on memory addresses having a predetermined address length ~~of m1 bits~~; and"

- **The 1st paragraph of Claim 2 is now amended to be**:

"The chip according to claim 1, wherein the data comprise data words having a predetermined word length ~~of m_2 bits~~ stored at each address, such that the second bus has a bus width smaller than the predetermined word length ~~m_2~~, and"

- **Claim 3 is now amended to be**:

"The chip according to claim 2, wherein the data words comprise data values for processing by the ~~device~~ processing component, and wherein the processing component is arranged to load the compacted data words via the second bus from the cache for processing and to store the compacted data words via the second bus to the cache."

- **Claim 4 is now amended to be**:

"The chip according to claim 2, wherein the data words comprise instructions for execution by the ~~device~~ processing component, wherein the compacted words comprise compacted instructions, and wherein the processing component is arranged to fetch the compacted instructions via the second bus."

- **The 2nd and 3rd paragraphs of Claim 14 is now amended to be**:

"configuring the Level 1 and Level 2 caches to store data for use by the processing component responsively to an addressing scheme based on memory addresses having a predetermined address length ~~of m_1 bits~~;

coupling first and second buses on the chip between the processing component and the L1 cache, and third and fourth buses on the chip coupled between the L1 cache and the L2 cache, the first and third buses having bus widths smaller than the predetermined address length ~~m_1~~;"

- **The 1st paragraph of Claim 15 is now amended to be**:

"The method according to claim 14, wherein the data comprise data words having a predetermined word length ~~of m_2 bits~~ stored at each address, such that the second bus has a bus width smaller than the predetermined word length ~~m_2~~, and"

Allowable Subject Matter

5. Claims 1-12 and 14-25 are allowed.

Reasons for Allowable

6. The following is an Examiner's statement of reasons for allowance:

Independent claims 1 and 14 recite, among other features, the particular limitation of "**wherein the L1 cache comprises a table for use in compaction of address fields that is shared by the address bus expanders coupled to the first and third buses.**"

None of the prior art of the record teaches or suggests, independently or in combination, this specific limitation recited by independent claims 1 and 14.

Conclusion

7. Claims 1-12 and 14-25 are allowed.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4178. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

November 28, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
11/29/06